In the Claims

Please amend the claims as follows:

1. A semiconductor processing method of forming transistors comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron, at least two of the widths being different; and

forming a gate line over respective active areas to provide individual transistors, the transistors corresponding to the active areas having the different widths having different threshold voltages.

2. The semiconductor processing method of claim 1 further comprising for the transistors having the different widths, providing the different threshold voltages without using a separate channel implant for the transistors.

3. The semiconductor processing method of claim 1, wherein the two different widths are each less than one micron.

4. The semiconductor processing method of claim 1, wherein the different threshold voltages are each less than 2 volts.

5. The semiconductor processing method of claim 1, wherein the different threshold voltages are each less than 1 volt.

6. The semiconductor processing method of claim 1, wherein the two different widths are each less than one micron, and the different threshold voltages are each less than 2 volts.

7. The semiconductor processing method of claim 1, wherein the two different widths are each less than one micron, and the different threshold voltages are each less than 1 volt.

51. The method of claim 1, wherein forming individual transistors comprises forming at least one active area of one of the transistors to have a width less than one micron.

52. The method of claim 1, wherein forming individual transistors comprises forming three individual transistors, a first of the three having a first threshold voltage, a second of the three having a second threshold voltage greater than the first threshold voltage and a third of the three having a third threshold voltage greater than the second threshold voltage.

53. (Amended) The method of claim 1, wherein forming individual transistors comprises forming at least three individual transistors, a first of the three having a first threshold voltage, a second of the three having a second threshold voltage greater than the first threshold voltage and a third of the three having a third threshold voltage greater than the second threshold voltage, the three individual transistors being configured to be coupled in parallel.

54. A semiconductor processing method of forming transistors comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths over the substrate, at least two of the widths being different, at least one of the plurality of active areas having a width less than one micron;

forming a gate line over respective active areas to provide individual transistors having different threshold voltages, the transistors being provided with the different threshold voltages without using separate channel implants; and

wherein a transistor with a lower one of the threshold voltages corresponds to the active area having the width less than one micron.

55. The method of claim 54 further comprising forming a transistor having a higher one of the threshold voltages to have an active area width greater than one micron.

56. The method of claim 54 further comprising forming a transistor having one of a higher of the threshold voltages to have an active area width less than one micron.

57. The method of claim 54 further comprising conducting only one common channel implant for the plurality of transistors.

58. The method of claim 54, wherein the forming of the gate line comprises forming a common gate line over the plurality of active areas.

59. The method of claim 54, wherein forming the gate line comprises forming a common gate line over the plurality of active areas, the transistors being formed in a parallel configuration.

60. The method of claim 54, wherein the different threshold voltages are each less than 1 volt.

61. The method of claim 54, wherein the at least two of the different widths are each less than one micron, and the different threshold voltages are all less than 2 volts.

62. The method of claim 54, wherein at least two of the different widths are each less than one micron, and the different threshold voltages are all less than 1 volt.

63. A semiconductor processing method of forming transistors comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron, at least two of the widths being different; and

forming a gate line over respective active areas to provide individual transistors, the transistors corresponding to the active areas having the different widths having different threshold voltages without using a separate channel implant for the transistors, wherein the different threshold voltages are each less than 2 volts, wherein forming a plurality of shallow trench isolation regions comprises forming at least one active area of one of the transistors to have a width less than one micron.

64. The semiconductor processing method of claim 63, wherein the at least two different widths are less than one micron.

65. The semiconductor processing method of claim 63, wherein the different threshold voltages are each less than 1 volt.

66. (Amended) The semiconductor processing method of claim 63, wherein the at least two different widths are less than one micron, and the different threshold voltages are less than 1 volt.

New Claims

67. A semiconductor processing method of forming transistors comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths over the substrate, at least two of the widths being different, at least one of the plurality of active areas having a width less than one micron;

forming a gate line over respective active areas to provide individual transistors having different threshold voltages, the transistors being provided with the different threshold voltages without using separate channel implants, wherein forming the gate line comprises forming a common gate line over the plurality of active areas, the transistors being formed in a parallel configuration; and

wherein a transistor with a lower one of the threshold voltages corresponds to the active area having the width less than one micron.

68. The method of claim 67 further comprising forming a transistor having a higher one of the threshold voltages to have an active area width greater than one micron.

69. The method of claim 67 further comprising forming a transistor having one of a higher of the threshold voltages to have an active area width less than one micron.

70. The method of claim 67 further comprising conducting only one common channel implant for the plurality of transistors.

71. The method of claim 67, wherein the forming of the gate line comprises forming a common gate line over the plurality of active areas.

72. The method of claim 67, wherein the different threshold voltages are each less than 1 volt.

73. The method of claim 67, wherein the at least two of the different widths are each less than one micron, and the different threshold voltages are all less than 2 volts.

74. The method of claim 67, wherein forming individual transistors comprises forming at least three individual transistors, a first of the three having a first threshold voltage, a second of the three having a second threshold voltage greater than the first threshold voltage and a third of the three having a third threshold voltage greater than the second threshold voltage, the three individual transistors being configured to be coupled in parallel.